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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/584,705

06/23/2006

Aviral Mittal

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05/22/2008

NXP, B.V.

NXP INTELLECTUAL PROPERTY DEPARTMENT

M/S41-SJ

1109 MCKAY DRIVE

SAN JOSE, CA 95131

EXAMINER

KERVEROS, JAMES C

ART UNIT

PAPER NUMBER

2117

NOTIFICATION DATE

DELIVERY MODE

05/22/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/584,705	<b>Applicant(s)</b> MITTAL, AVIRAL	
	<b>Examiner</b> JAMES C. KERVEROS	<b>Art Unit</b> 2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 June 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

This is a non-Final Office Action in response to the PRELIMINARY AMENDMENT filed 6/23/2006. The present US Application 10/584705, filed 06/23/2006, is a national stage entry of PCT/IB04/52847, international Filing Date: 12/17/2004.

#### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), for UNITED KINGDOM Application No. 0330076.1, filed 12/27/2003, which papers have been placed of record in the file.

Claims 1-15 are presently under examination and pending.

#### ***Drawings***

The drawings are objected to under 37 CFR 1.83(a) because they fail to show the functional descriptive legends corresponding to blocks 10, 16, 22, 18, 26 for Figs. 1 and 3, as described in the specification. Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing. They should contain as few words as possible.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 and 15 recite in the preamble the limitation “arranged such that the rising edges of the second of the clock pulses are aligned”, which renders the claims indefinite, because it is unclear whether the limitations following the phrase “such that” are part of the claimed invention. Also, it is not clear how in relation to what clock or signal, “the rising edges of the second of the clock pulses are aligned”.

Claims 1 and 14 recite the limitation “both input clock signals”, which lack antecedent basis. It appears from the claimed language “both input clock signals” are the same as the previously recited “two respective clock signals”.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Nadeau-Dostie et al. (US Patent No. 6,510,534), issued: January 21, 2003.

Regarding independent Claims 1, 14, Nadeau-Dostie discloses a method and apparatus for testing high performance circuits, comprising:

A BIST controller 20 including a clock generation module 42 for generating two clock pulses (CaptureCLK) during a capture sequence following a shift sequence in response to a system clock (SystemCLK) and a (BistCLK) having different frequencies, as shown in Figs. 3-6.

Fig. 4 illustrates a more detail diagram of the clock generation module 42, which includes a delay circuit 64 which produces a capture clock control signal SED, shown as ScanEnableDelayed in Fig. 6, and a transition detector circuit 60, which generates a capture clock enable signal, EN.

When at-speed testing is enabled, when both Init and Debug are inactive, the capture clock is obtained by gating the output of a transition detector circuit 60, which detects a falling transition on a delayed version of the ScanEnable signal, and the system clock by means of an AND gate 62.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US Patent No. 6,510,534).

Regarding Claims 2-13 and 15, Nadeau-Dostie does not explicitly disclose the claimed design configuration of threshold values comprising functions of the ratio of the fastest clock frequency to the clock frequency for generating the two clock pulses. However, Nadeau-Dostie utilizes logic gating design, which is an alternative design well known in the art for generating the two clock pulses (CaptureCLK) during the capture sequence. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use alternative design means for the purpose of generating two clock pulses during at-speed testing. A person skilled in the art would have been motivated to do so, since Nadeau-Dostie takes into consideration the frequency ratio, which will work well for any frequency ratio greater than four. This is typical for high-performance circuits. If a lower frequency ratio is required and the test clock frequency cannot be changed, the effective shift clock frequency must be reduced to

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maintain a frequency ratio greater than four with respect to the capture clock frequency.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/  
Primary Examiner, Art Unit 2117

Date: 20 May 2008  
Office Action: Non-Final Rejection

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